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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,576	09/05/2003	Cheon Hong Kim	CU-3351 RJS	7892
26530	7590	06/08/2007		
LADAS & PARRY LLP 224 SOUTH MICHIGAN AVENUE SUITE 1600 CHICAGO, IL 60604			EXAMINER LIANG, REGINA	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 06/08/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/656,576	<b>Applicant(s)</b> KIM ET AL.	
	<b>Examiner</b> Regina Liang	<b>Art Unit</b> 2629	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 April 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1, 2 and 4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

1. The finality of that action mailed 2/7/07 is withdrawn. Claims 1, 2 and 4 are pending in the application.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al (US 4,621,260 hereinafter Suzuki).

As to claim 1, Figs. 2 and 3 of Suzuki discloses a liquid crystal display comprising:

thin film transistors (20) connected to intersections between a plurality of data lines (Y1-Yn) and a plurality of gate lines (X1-Xm);

pixel electrodes (22), each of which is connected to a source (34) of each of the thin film transistors (20);

common electrodes opposed to the pixel electrodes;

liquid crystal injected between the pixel electrodes and the common electrodes;

a plurality of auxiliary gate lines (Z1-Zm), each of said auxiliary gate lines having a signal with a polarity that is opposite to the polarity of a signal on a corresponding gate line (col. 5, lines 30-32 and Figs. 4A, 4C);

first capacitors (28), each of which is connected between the source and each of the auxiliary gate lines;

wherein the polarity of the voltage applied to the auxiliary gate line is opposite to that applied to the gate line (col. 5, lines 30-32, and Figs. 4A and 4C).

As to claim 2, Suzuki teaches the liquid crystal display having a second capacitor (26) is connected between the source and each of the common electrodes (it is inherent the common electrode is connected to ground).

As to claim 4, Suzuki teaches the first capacitor (28) has capacitance (Cz) identical to that of parasitic capacitance (Cp) between the source and gate of the thin film transistor (see col. 1-17, set  $\Delta v=0$ , then  $C_p=C_z$ ).

#### ***Claim Rejections - 35 USC § 103***

5. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US Patent No. 4,393,405) in view of Ozawa et al. (US Patent No. 6,839,045)

As to claim 1, Ikeda discloses a liquid crystal display (Fig. 1) comprising: thin film transistors (102) connected to intersections between a plurality of data lines (D1...Dn) and a plurality of gate lines (G1...Gm); pixel electrodes (e.g., top portion electrode of the LCD cell 104), each of which is connected to a source of each of the thin film transistors; common electrodes (e.g. bottom portion electrode of the LCD cell 104) opposed to the pixel electrodes; liquid crystal (104) injected between the pixel electrodes and the common electrodes. It is noted

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that Ikeda does not disclose a plurality of auxiliary gate lines corresponding to the gate lines, and first capacitors, each of which is connected between the source and each of the auxiliary gate lines.

Ozawa is cited to teach an active matrix flat panel display similar to Ikeda. Ozawa further discloses a plurality of auxiliary gate lines (e.g. cline line as shown in Fig. 2), each of the auxiliary data lines having a signal with a polarity that is opposite to the polarity of a signal on a corresponding gate lines and the polarity of the voltage applied to the auxiliary gate line is opposite to that applied to the gate line (col. 25, line 48 to col. 26, line 3 for example), and first capacitors (e.g. cap as shown in Fig. 2), each of which is connected between the source and each of the auxiliary gate lines (see Fig. 2). It would have been obvious to one of ordinary skill in the art to have modified Ikeda with the features of the auxiliary gate lines as taught by Ozawa because the capacitor connected to the auxiliary gate line can maintain the pixel voltage even the transistor is turned "off" (see col. 9, lines 50-67).

As to claim 2, Ikeda as modified discloses a second capacitor (103) is connected between the source and each of the common electrodes (e.g. the capacitor 103 is connected to the common electrode of the pixel in the same common line as shown in Fig. 1).

### ***Response to Arguments***

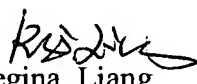
6. Applicant's arguments with respect to claims 1, 2 and 4 have been considered but are moot in view of the new ground(s) of rejection.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Regina Liang  
Primary Examiner  
Art Unit 2674

6/4/07